

1. General Description

This 8-bit Micro-controller uses a fully static CMOS technology to achieve high speed, small size, low power and high noise immunity.

2. Features

- ◆ Fully CMOS static design
- ◆ 8-bit data bus
- ◆ 37 single word instructions
- ◆ 14-bit instructions
- ◆ 8-level stacks
- ◆ Operating voltage : 2.3V ~ 5.5 V
- ◆ Watchdog timer with on-chip RC oscillator
- ◆ Interrupt capability
- ◆ Timer0 : 8-bit timer with 3-bit prescaler
- ◆ Timer1 : 16-bit timer with 2-bit prescaler
- ◆ Analog comparator module
- ◆ Sleep mode for power saving
- ◆ PA with port change wake-up interrupt
- ◆ Power-on Reset
- ◆ I/O pins with their own independent direction control

3. Applications

The application areas of this range from appliance motor control and high speed automotive to low power remote transmitters/receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral ... etc.

4. Pin Assignment

CYICT90F630P11/S11

VDD	1	14	VSS
OSC1/PA5	2	13	PA0/CIN+
OSC2/PA4	3	12	PA1/CIN-
PA3	4	11	PA2/INT
PC5	5	10	PC0
PC4	6	9	PC1
PC3	7	8	PC2

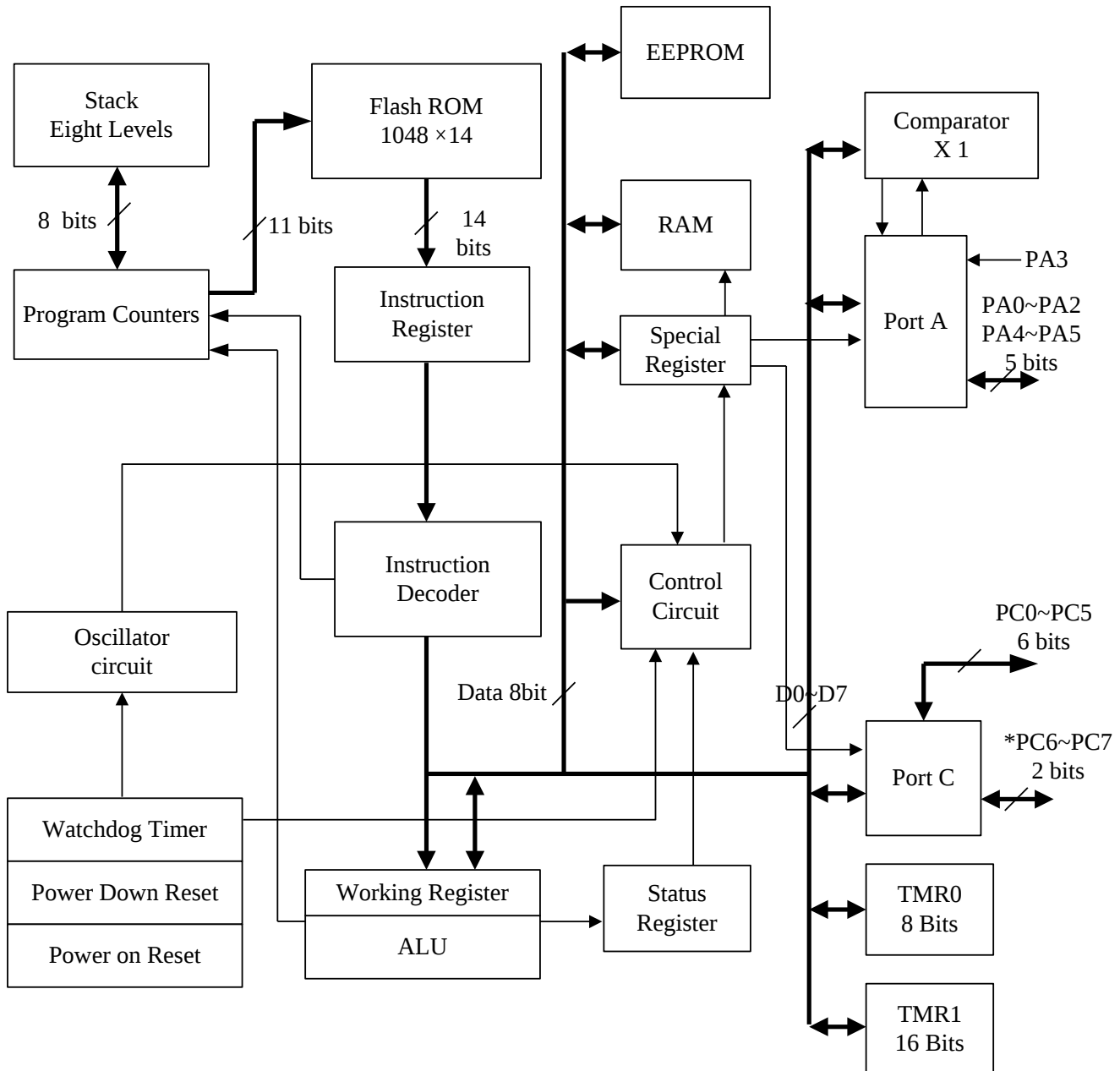
CYICT90F6301P11/S11

PC6	1	16	PC7
VDD	2	15	VSS
OSC1/PA5	3	14	PA0/CIN+
OSC2/PA4	4	13	PA1/CIN-
/PA3	5	12	PA2/INT
PC5	6	11	PC0
PC4	7	10	PC1
PC3	8	9	PC2

5. Order Information

Device	ROM (Words)	RAM (Bytes)	EEPROM (Bytes)	I/O	Comparators	Timer (8/16 bit)	Package	REMARK
CYICT90F630P11	1.0K	64	128	11	1	1/1	14 DIP	PIN4 IS PA3 FUNC.
CYICT90F630S11	1.0K	64	128	11	1	1/1	14 SOP	
CYICT90F6301P11	2.0K	96	128	13	1	1/1	16 DIP	
CYICT90F6301S11	2.0K	96	128	13	1	1/1	16 SOP	

6. Block Diagram



* 90F6301 only

**7. Pin Function Description**

Pin name	Type	Buffer type	Description	
PA0/C1+IN	I/O	TTL	TTL input level , with program pull_hi and interrupt on pin change.	Comparator1 + input..
PA1/C-IN	I/O	TTL		Comparator – input..
PA2/T0CK/INT/ COUT	I/O	TTL		Timer0 clock input. External interrupt. Comparator1 output.
MCLRB/PA3	I	TTL/ ST	TTL input level, with program interrupt on pin change.	Master clear. Schmitt Trigger input level.
PA4/OSC2/T1GB	I/O	TTL/ ST	TTL input level , with program pull_hi and interrupt on pin change.	Oscillator crystal output, in RC mode clock output Fosc/4 frequency. Timer1 gate. Schmitt Trigger inputlevel
PA5/OSC1/T1CKI	I/O	TTL/ST		Oscillator crystal input/external clock source input. Timer1 clock input. Schmitt Trigger input level.
PC0	I/O	TTL	TTL input level.	
PC1	I/O	TTL		
PC2	I/O	TTL		
PC3	I/O	TTL		
PC4	I/O	TTL		
PC5	I/O	TTL		
*PC6	I/O	TTL		
*PC7	I/O	TTL		
Vdd			Power supply	
Vss			Ground	

* 90F6301 only

**8. Memory Map****8.1 Program memory :**

0000H	Reset Vector
0001H	
0002H	
0003H	
0004H	Peripheral interrupt Vector
0005H	Program Memory
03FFH	
0400H	
07FFH	* Program Memory

* 0400H~07FFH : 90F6301 only



8.2 Register file map :

90F630

ADDR	BAK0	BAK1	ADDR
00H	IADD	IADD	80H
01H	TMR0	OPTR	81H
02H	PCL	PCL	82H
03H	STATUS	STATUS	83H
04H	RSR	RSR	84H
05H	PORTA	PTIO A	85H
06H			86H
07H	PORTC	PTIO C	87H
08H			88H
09H			89H
0AH	PCH	PCH	8AH
0BH	INTCTL	INTCTL	8BH
0CH	PIF1	PIE1	8CH
0DH			8DH
0EH	TMR1L	PWCTL	8EH
0FH	TMR1H		8FH
10H	T1CTL	EOSCCTL	90H
11H			91H
12H			92H
13H			93H
14H			94H
15H		PAPHR	95H
16H		PAINTR	96H
17H			97H
18H			98H
19H	CMCTL	VRCTL	99H
1AH		EEDATA	9AH
1BH		EEADR	9BH
1CH		EECTL1	9CH
1DH		EECTL2	9DH
1EH			9EH
1FH			9FH
20H	Genreal register 64 byte	Mapping 20H ~ 5FH	A0H
5FH			DFH
60H			
7FH			7FH

90F6301

ADDR	BAK0	BAK1	ADDR
00H	IADD	IADD	80H
01H	TMR0	OPTR	81H
02H	PCL	PCL	82H
03H	STATUS	STATUS	83H
04H	RSR	RSR	84H
05H	PORTA	PTIO A	85H
06H			86H
07H	PORTC	PTIO C	87H
08H			88H
09H			89H
0AH	PCH	PCH	8AH
0BH	INTCTL	INTCTL	8BH
0CH	PIF1	PIE1	8CH
0DH			8DH
0EH	TMR1L	PWCTL	8EH
0FH	TMR1H		8FH
10H	T1CTL	EOSCCTL	90H
11H			91H
12H			92H
13H			93H
14H			94H
15H		PAPHR	95H
16H		PAINTR	96H
17H			97H
18H			98H
19H	CMCTL	VRCTL	99H
1AH		EEDATA	9AH
1BH		EEADR	9BH
1CH		EECTL1	9CH
1DH		EECTL2	9DH
1EH			9EH
1FH			9FH
20H	Genreal register 96 byte	Mapping 20H ~ 7FH	A0H
7FH			FFH



Unimplemented memory location.



CYICT90F630/90F6301 REGISTER FILE SUMMARY

Address	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BANK0									
00	IADD	Addressing this location uses the content of RSR to address data memory (not a physical register)							
01	TMR0	8 Bit Real time clock / counter							
02	PCL	Low order 8 bit of PC							
03	STATUS	-	-	RPS0	/TO	/PL	Z	HC	C
04	RSR	Indirect Register Address pointer							
05	PORT A	-	-	PA5	PA4	PA3	PA2	PA1	PA0
07	PORT C	*PC7	*PC6	PC5	PC4	PC3	PC2	PC1	PC0
0A	PCHLAT	Write buffer for high byte of PC							
0B	INTS	GIE	PEIE	T0IE	INTIE	PAIE	T0IF	INTIF	PAIF
0C	PIF1	EEIF	-	-	-	CMIF	-	-	TMR1IF
0E	TMR1L	Timer 1 Least Significant Byte							
0F	TMR1H	Timer 1 Most Significant Byte							
10	T1CTL	-	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	/T1SYNC	TMR1CLK	TMR1ON
19	CMCTL	-	CMOUT	-	CMOINV	CMIS	CMP2	CMP1	CMP0
BANK1									
81	OPTR	PAPH	INTES	T0CS	T0SE	PSS	PS2	PS1	PS0
85	PTIO A	-	-	PORTA		DATA	DIRECTION	REGISTER	
87	PTIO C	*PTIOPC7	*PTIO PC6	PTIO PC5	PTIO PC4	PTIO PC3	PTIO PC2	PTIO PC1	PTIO PC0
8C	PIE1	EEIE-	-	-	-	CMIE	-	-	TMR1IE
8E	PWCTL	-	-	-	-	-	-	PORB	-
90	EOSCCTL	ENINF	-	-	EN8M	ECKIN	OSO2E	OSC2O	OSCIN
95	PAPHR	-	-	PAH5	PAH4	-	PAH2	PAH1	PAH0
96	PAINTR	-	-	PINTA5	PINTA4	PINTA3	PINTA2	PINTA1	PINTA0
99	VRCTL	CVRE	-	CVRRS	-	CVR3	CVR2	CVR1	CVR0
9A	EEDATA	EEPROM DATA REGISTER							
9B	EEADR	EEPROM ADDRESS REGISTER							
9C	EECTL1	-	-	-	-	WRERR	WREN	WR	RD
9D	EECTL2	EEPROM control		Register 2					

00H、80H、100H、180H : IAR (Indirect Address Register)

Use contents of RSR to address data memory (not a physical register)

* 90F6301 only

(1).01H : TMR0 (Timer0 Counter).

8-bit real time clock/counter

(2).02H、82H : PCL (Program Counter Low Byte)

Low order 8 bits of the Program Counter (PC)

(3).03H、83H、: STATUS (Status register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	-	-	RPS0	/TO	/PL	Z	HC	C



Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	/PL	Power loss Flag bit
4	/TO	WDT TIME OUT bit
5	RPS0	Register page select bit 0 0 : 00/H --- 7F/H 0 1 : 80/H --- FF/H

(4).04H、84H : RSR (Memory Select Register)

Indirect data memory address pointer.

(5).05H、105H : Port A data output register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port A	-	-	PA5	PA4	PA3	PA2	PA1	PA0

Bit 7 – 6 : Unimplemented

Bit 5 – 0 : PA5 ~ PA0 , I/O Register

(6).07H: Port C data output register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port C	*PC7	*PC6	PC5	PC4	PC3	PC2	PC1	PC0

* 90F6761 only

(7).08 ~ 09H : Unimplemented Register.

(8).0AH、8AH: Program counter high byte.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCHLAT	-	-	-	PCH4	PCH3	PCH2	PCH1	PCH0

(9). 0BH、8BH : Interrupt control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTS	GIE	PEIE	T0IE	INTIE	PAIE	T0IF	INTIF	PAIF



Bit	Symbol	Function
0	PAIF	PA Port Change Interrupt Flag Bit. 0 = None of the PA pins have changed state 1 = When at least one of the PA pins changed state (must be cleared in software)
1	INTF	PA2/INT Interrupt Flag Bit. 0 = The PA2/INT interrupt did not occur 1 = The PA2/INT interrupt occurred
2	T0IF	TMR0 Overflow Interrupt Flag Bit. 0 = Timer0 did not overflowed 1 = Timer0 has overflowed (must be cleared in software)
3	PAIE	PA Port Change Interrupt Enable Bit. 0 = disable PA,PB change interrupt 1 = enable PA,PB change interrupt
4	INTIE	INT Pin Interrupt Enable Bit. 0 = disable INT interrupt 1 = enable INT interrupt
5	T0IE	TMR0 Overflow Interrupt Enable Bit. 0 = disable TMR0 interrupt 1 = enable TMR0 interrupt
6	PEIE	Peripheral Interrupt Enable Bit. 0 = disable all peripheral interrupt 1 = enable all peripheral interrupt
7	GIE	Global Interrupt Enable Bit. 0 = disable global interrupt 1 = enable global interrupt

(10). 0CH : PIF1 (Peripheral interrupt register1).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIF1	EEIF	-	-	-	-	-	-	TMR1IF

Bit	Symbol	Function
0	TMR1IF	TMR1 Overflow Interrupt Flag Bit. 0 = Timer1 register did not overflow 1 = Timer1 register overflowed (must be cleared in software)
1~6	-	-
7	EEIF	EE interrupt flag bit. 0 = EE operation has not completed 1 = EE operation has completed

(11). 0EH : TMR1L (The timer1 LSB register)
The LSB of the 16-bit TMR1.



- (12). 0FH : TMR1H (The timer1 MSB register)
The MSB of the 16-bit TMR1.

- (13). 10H : Timer1 control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1CTL		TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	/T1SYNC	TMR1CLK	TMR1ON

Bit	Symbol	Function
0	TMR1ON	0 = Stop TMR1 1 = Enable TMR1
1	TMR1CLK	0 = Internal clock (Fosc/4) 1 = External clock from pin PA5
2	$\overline{\text{T1SYNC}}$	TMR1CLK = 1 0 = Synchronize external clock 1 = Do not synchronize external clock TMR1CLK = 0 This bit is ignored
3	T1OSCEN	If INTOSC without CLKOUT oscillator is active : 0 = LP oscillator is off 1 = LP oscillator is enabled for Timer1 clock
4~5	T1CKPS1 ~ T1CKPS0	0 0 = 1 : 1 Prescale value 0 1 = 1 : 2 Prescale value 1 0 = 1 : 4 Prescale value 1 1 = 1 : 8 Prescale value
6	TMR1GE	TMR1 gate control enable bit TMR1ON = 0 , this bit is ignored TMR1ON = 1 , 0 : gate control disable 1 : gate control enable
7	-	-

- (14). 11 ~ 18H : Unimplemented register.

- (15). 19H : CMCTL(Comparator control register.)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMSTA	-	CMOUT	-	CMOINV	CMIS	CMP2	CMP1	CMP0



Bit	Symbol	Function
2~0	CMP0 ~ CMP2	Comparator Mode Bits. 0 0 0 = Comparator reset– low power(default) 0 0 1 = Comparator with output 0 1 0 = Comparator without output 0 1 1 = Comparator with output and internal reference (cvref . see 99H register) 1 0 0 = Comparator without output and with internal reference (cvref . see 99H register) 1 0 1 = Comparator multiplexed input with internal referenceand output (cvref . see 99H register) 1 1 0 = Comparator multiplexed input with internal reference (cvref . see 99H register) 1 1 1 = Comparator off (lowest power)
3	CMIS	Comparator input switch bit.(CMP2~0=110 or 101) 0 = Vin- connects to CIN- 1 = Vin- connects to CIN+
4	CMOINV	Comparator output Inversion Bit 0 = Output not inverted 1 = Output inverted
5	-	-
6	CM1OUT	Comparator Output Bit. When CMOINV = 0 1 = Vin+ > Vin- ; 0 = Vin+ < Vin- When CMOINV = 1 1 = Vin+< Vin- ; 0 = Vin+ > Vin-
7	-	-

(16). 1A ~ 1DH : Unimplemented register.

(17). 81H : OPTR (Option control register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTR	/PAPH	INTES	T0CS	T0SE	PSS	PS2	PS1	PS0



Bit	Symbol	Function		
2~0	PS2 ~ PS0	Prescaler Value	TMR0 rate	WDT rate
		0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSS	Prescaler assignment bit : 0 = Timer 0 1 = Watchdog Timer		
4	T0SE	TMR0 signal Edge : 0 = Increment on low-to-high transition on PA2 pin 1 = Increment on high-to-low transition on PA2 pin		
5	T0CS	TMR0 signal set : 0 = Internal instruction cycle clock 1 = Transition on PA2/INT pin		
6	INTES	PA2 interrupt edge select bit : 0 = Interrupt on falling edge of PA2/INT pin 1 = Interrupt on rising edge of PA2/INT pin		
7	/PAPH	Port A Pull-up Enable Bit : 0 = PA0~2 & PA4~5 pull-up all enable 1 = PA0~2 & PA4~5 pull-up all disable		

(18). 85H : Port A input/output control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PTIO A	-	-	PTIO PA5	PTIO PA4	PTIO PA3	PTIO PA2	PTIO PA1	PTIO PA0

(19). 87H : Port C input/output control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PTIO C	*PTIO PC7	*PTIO PC6	PTIO PC5	PTIO PC4	PTIO PC3	PTIO PC2	PTIO PC1	PTIO PC0

* 90F6301 only

(20). 88H ~ 89H : Unimplemented register.



(21). 8CH : PIE1 (Peripheral interrupt enable register1).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIE1	EEIE	-	-	-	-	-	-	TMR1IE

Bit	Symbol	Function
0	TMR1IE	TMR1 Overflow Interrupt Enable Bit. 0 = Disable the TMR1 overflow interrupt 1 = Enable the TMR1 overflow interrupt
6~1	-	-
7	EEIE	EEPROM Write Operation Interrupt Enable Bit. 0 = Disable the EEPROM write complete interrupt 1 = Enable the EEPROM write complete interrupt

(22). 8EH : PWCTL (Power control register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWCTL	-	-	-	-	-	-	PORB	-

PORB : Power On Reset Status Bit.

0 = A power on reset occurred

(must be set in software after a power on reset occurs)

1 = No power on reset occurred

(23). 90H : EOSCCTL (external oscillator control register.)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EOSCCTL	ENINF	-	-	EN8M	ECKIN	OSO2E	OSC2O	OSCIN



Bit	Symbol	Function
0	OSCIN	MCU Internal or external oscillator Select Bit. 0 = MCU clock based on internal oscillator(default) 1 = MCU clock based on external oscillator (type from option select) When internal oscillator change to external oscillator must wait OST time 20ms.
1	OSC2O	OSC2 Oscillator Clock Output Enable Bit. 0 = Disable OSC2 oscillator clock output in internal or external of RC mode oscillator 1 = Enable OSC2 oscillator clock output in internal or external of RC mode oscillator
2	OSO2E	Both of highspeed-Internal and external oscillator Enable Bit. 0 = Only use internal oscillator or external oscillator 1 = Internal and external (LF mode only) oscillator enable both
3	ECKIN	External Clock Input Enable Bit. 0 = Disable oscillator external clock input 1 = Enable oscillator external clock input (must be set in external oscillator of RC mode)
4	EN8M	INTRC change to 8MHz 0 = IRC use 4MHz(default) 1 = IRC use 8MHz
6~5	-	-
7	ENINF	Enable internal RC flag Bit.

91H ~ 94H : Unimplemented register.

(24). 95H : PAPHR (Port A pull_hi control register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAPHR	-	-	PHA5	PHA4	-	PHA2	PHA1	PHA0

Bit 5-4 & Bit 2-0 : Port A Pull_hi Control Bits

0 = Pull_hi disable

1 = Pull_hi enable



(25). 96H : PAINTR (Port A interrupt-on-change control register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAINTR	-	-	PINTA5	PINTA4	PINTA3	PINTA2	PINTA1	PINTA0

Bit 5-0 : Port A Interrupt-On-Change Control Bits

0 = Interrupt-on-change disable

1 = Interrupt-on-change enable

(26). 99H : VRCTL (Voltage reference control register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VRCTL	CVRE		CVRRS		CVR3	CVR2	CVR1	CVR0

Bit	Symbol	Function
3~0	CVR3 ~ CVR0	Comparator Voltage Reference Value Selection When CVRRS = 0, CVref = $V_{dd}/4 + (CVR3:CVR0/32)*V_{dd}$ When CVRRS = 1, CVref = $(CVR3:CVR0/24)*V_{dd}$
4	-	-
5	CVRRS	Comparator Voltage Reference Range Select Bit 0 = High range ; CVref = $V_{dd}/4 + (CVR3:CVR0/32)*V_{dd}$ 1 = Low range ; CVref = $(CVR3:CVR0/24)*V_{dd}$
6	-	-
7	CVRE	Comparator Voltage Reference Enable Bit 0 = Comparator voltage reference disable 1 = Comparator voltage reference enable

(27). 9AH : EEDATA (EEPROM data register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEDATA	EED7	EED6	EED5	EED4	EED3	EED2	EED1	EED0

(28). 9BH : EEADR (EEPROM address register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEADR	EEAD7	EEAD6	EEAD5	EEAD4	EEAD3	EEAD2	EEAD1	EEAD0



(29). 9CH : EECTL1 (EE control 1).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EECTL1	-	-	-	-	WRERR	WREN	WR	RD

Bit	Symbol	Function
0	RD	Read Control Bit. 0 = Does not initiate an EEPROM read. 1 = Initiates an EEPROM read (read takes once cycle. RD is cleared in hardware. The RD bit can only be set (not clear) in software.)
1	WR	Write Control Bit. 0 = Write cycle to the data EEPROM is complete 1 = Initiates a write cycle. (The bit is cleared by hardware once write is complete. The WR bit can only be set (not clear) in software.)
2	WREN	EEPROM Write Enable Bit. 0 = Inhibits write to the data EEPROM 1 = Allows write cycles
3	WRERR	EEPROM Write Error Flag Bit. 0 = The EEPROM write operation completed 1 = The EEPROM write operation is prematurely terminated (any MCLR reset or any WDT reset during normal operation)
7~4	-	-

(30). 9DH : EECTL2 (EE control 2).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EECTL2	-	-	-	-	-	-	-	-

Write only ; Read as "0"

When write data to the EEPROM must write 55/H to EECTL2,
and writ AA/H to EECTL2 then set WR bit;
the EEPROM can write data inside for write each byte.

Example : Data EEPROM Write



BSM STATUS, RPS0
 BCM INTS, GIE ; Disable interrupt
 BSM EECTL1, WREN ; Enable write
 MOVKW 55H
 MOVWM EECTL2 ; Write 55/H
 MOVKW 0AAH
 MOVWM EECTL2 ; Write AA/H
 BSM EECTL1,WR ; Begin write

9. Reset Condition for all Registers

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IADD	00h(80h)	0000 0000	0000 0000	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h(82h)	0000 0000	0000 0000	0000 0100
STATUS	03h(83h)	0001 1xxx	000# #uuu	000# #uuu
RSR	04h(84h)	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	--xx xxxx	--uu uuuu	--uu uuuu
PORT C	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCHLAT	0Ah(8Ah)	---0 0000	---0 0000	---u uuuu
INTS	0Bh(8Bh)	0000 0000	0000 0000	uuuu uuuu
PIF1	0Ch	0--- 0--0	0--- 0--0	u--- u--u
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CTL	10h	-000 0000	-000 0000	-uuu uuuu
CMCTL	19h	-0-0 0000	-0-0 0000	-u-u uuuu
OPTR	81h	1111 1111	1111 1111	uuuu uuuu
PTIO A	85h	--11 1111	--11 1111	--uu uuuu
PTIO C	87h	1111 1111	1111 1111	uuuu uuuu
PIE1	8Ch	0--- 0--0	0--- 0--0	u--- u--u
PWCTL	8Eh	---- --#-	---- --u-	---- --u-
EOSCCTL	90h	x--0 0000	x--0 0000	u--u uuuu
PAPHR	95h	--11 -111	--11 -111	--uu -uuu
PAINTR	96h	--00 0000	--00 0000	--uu uuuu
VRCTL	99h	0-0- 0000	0-0- 0000	u-u- uuuu
EEDATA	9Ah	0000 0000	0000 0000	uuuu uuuu
EEADR	9Bh	-000 0000	-000 0000	-uuu uuuu
EECTL1	9Ch	---- #000	---- #000	---- #uuu
EECTL2	9Dh	---- ----	---- ----	---- ----

Note1 : “x” = unknown; “u” = unchanged; “-” = unimplemented, read as “0”; “#” = value depends on condition

**10. Instruction Set**

Mnemonic Operands	Function	Operation	Status
NOP	No operation	None	
SELT	Load W to OPTR register	$W \rightarrow \text{OPTR}$	None
SLEEP	Sleep mode	$0 \rightarrow \text{WDT}$, stop OSC	/TO, /PL
WDTCLR	Clear Watchdog timer	$0 \rightarrow \text{WDT}$	/TO, /PF
PTIO M	Control I/O port register	$W \rightarrow \text{PTIO } M$	None
RET	Return from subroutine	$\text{Stack} \rightarrow \text{PC}$	None
RETI	Return from interrupt	$\text{Stack} \rightarrow \text{PC}, 1 \rightarrow \text{GIE}$	None
MOVWM M	Store W to Memory	$W \rightarrow M$	None
CLRW	Clear working register	$0 \rightarrow W$	Z
CLRM M	Clear Memory	$0 \rightarrow M$	Z
SUBWM M,t	Subtract W from Memory	$M - W \rightarrow t$ ($M+/W+1 \rightarrow t$)	C, HC, Z
DECM M,t	Decrement Memory	$M - 1 \rightarrow t$	Z
ORWM M,t	Inclu. OR W and Memory	$M \cup W \rightarrow t$	Z
ADDWM M,t	Add W and Memory	$W + M \rightarrow t$	C, HC, Z
XORWM M,t	Exclu. OR W and Memory	$M \oplus W \rightarrow t$	Z
ANDWM M,t	AND W and Memory	$M \cap W \rightarrow t$	Z
MOVM M,t	Load Memory	$M \rightarrow t$	Z
COMM M,t	Complement Memory	$/M \rightarrow t$	Z
INCM M,t	Increment Memory	$M + 1 \rightarrow t$	Z
DECMZS M,t	Decrement Memory, if zero skip next Memory	$M - 1 \rightarrow t$	None
RRCM M,t	Rotate right Carry bit and Memory	$M(n) \rightarrow M(n-1),$ $C \rightarrow M(7), M(0) \rightarrow C$	C
RLCM M,t	Rotate left Carry bit and Memory	$M(n) \rightarrow M(n+1),$ $C \rightarrow M(0), M(7) \rightarrow C$	C
SWAPM M,t	Swap halves Memory	$[M(0 \sim 3) \square M(4 \sim 7)] \rightarrow t$	None
INCMZS M,t	Increment Memory, if zero skip next Memory	$M + 1 \rightarrow t$	None
BCM M,b	Bit clear	$0 \rightarrow M(b)$	None
BSM M,b	Bit set	$1 \rightarrow M(b)$	None
BTZS M,b	Bit Test, if zero, skip next Memory	Skip if $M(b)=0$	None



Mnemonic Operands	Function	Operation	Status
BTSS M,b	Bit Test, if set,skip next Memory	Skip if M(b)=1	None
MOVKW I	Load immediate to W	I→W	None
RETKW I	Return, place immediate to W	Stack→PC, I→W	None
ORKW I	Inclu. OR immediate and W	$I \cup W \rightarrow W$	Z
ANDKW I	AND immediate and W	$I \cap W \rightarrow W$	Z
XORKW I	Exclu. OR immediate and W	$I \oplus W \rightarrow W$	Z
SUBKW I	Subtract W from immediate	$I - W \rightarrow W$	C,HC,Z
ADDKW I	ADD immediate and W	$I + W \rightarrow W$	C,HC,Z
CALL N	CALL subroutine	N→PC, PC+1→Stack	None
GOTO N	JUMP to address	N→PC	None

Note :

W	: Working register	b	: Bit position
WDT	: Watchdog timer	t	: Target. 0 : W 1 : M
OPTR	: OPTR register	M(m)	: General Memory address
PTIO	: Control I/O port register	C	: Carry flag
/TO	: Timer overflow flag	HC	: Half carry
/PL	: Power loss flag	Z	: Zero flag
PC	: Program Counter	/	: Complement
OSC	: Oscillator	x	: Don't care
Inclu.	: Inclusive '∪'	I(i)	: Immediate data
Exclu.	: Exclusive '⊕'	N(n)	: Immediate address
AND	: Logic AND '∩'		

**11. . Electrical Characteristics**

*Note: Temperature=25°C

Sym	Description	Condition		Min	Typ	Max	Unit
Vdd	Operating voltage			2.5		6.3	V
V _{IL}	Input Low Voltage	Vdd=5V		-0.6		1.0	V
V _{IH}	Input high Voltage PA, PC	Vdd=5V		2.0		Vdd	V
		Vdd=3V		1.5		Vdd	
I _{IL}	Input leakage current	Vdd=5V				+/-1	μA
V _{OL}	Output Low Voltage PA(ext PA3), PC	Vdd=5V, I _{OL} =20mA			0.59		V
		Vdd=5V, I _{OL} =5mA			0.2		V
V _{OH}	Output High Voltage PA(ext PA3), PC	Vdd=5V, I _{OH} = -20mA			3.2		V
		Vdd=5V, I _{OH} = -5mA			4.4		V
R _{ph}	PA(ext PA3) pullhigh resister	Vdd=5V			21k		Ω
		Vdd=3V			57k		
I _{slp}	Sleep current	V _{dd} = 2.5 V			1		μA
	OSC TYPE:IRC	V _{dd} = 3.0 V			1.6		μA
	PUT:75ms	V _{dd} = 4.0 V			3.7		μA
	WDT:Enable	V _{dd} = 5.0 V			6.5		μA
	PED:Disable	V _{dd} = 6.0 V			10.3		μA
I _{max}	Max output driver PA(ext PA3), PC	Vdd=5V	Sourse current		30		mA
			Sink current		50		
		Vdd=3V	Sourse current		10		mA
			Sink current		20		
I _{dd 1}	Operation Current 1 OSC TYPE:HF PUT:75ms WDT:Enable PED:Disable No load	4MHz	Vdd=5V		1.5		mA
			Vdd=3V		400		uA
		10MHz	Vdd=5V		2.0		mA
			Vdd=3V		750		uA
		20MHz	Vdd=5V		3		mA
			Vdd=3V		1.5		mA
I _{dd 2}	Operation Current 2 OSC TYPE:LF with 50p PUT:75ms WDT,PED:Disable No load	32KHz	V _{dd} = 2.5 V		15		uA
			V _{dd} = 3.0 V		20		uA
			V _{dd} = 5.0 V		90		uA

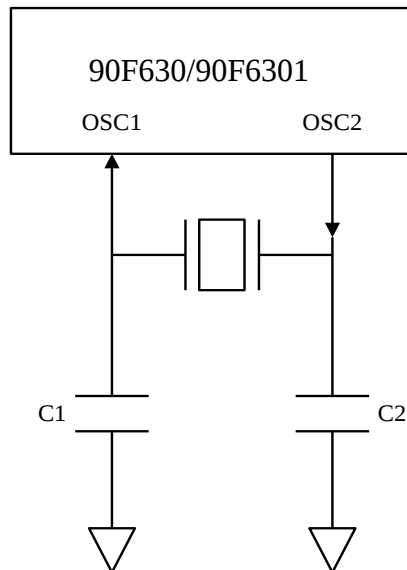


Sym	Description	Condition		Min	Typ	Max	Unit
Idd 3	Operation Current 3 OSC TYPE:RC PUT:0ms WDT,PED:Disable No load	4MHz	V _{dd} =5.0v		1.5		mA
			V _{dd} = 3.0		700		uA
		500kHz	V _{dd} =5.0v		300		uA
			V _{dd} = 3.0		100		uA
Idd 4	Operation Current 4 OSC TYPE:IRC PUT:0ms WDT,PED:Disable No load	4MHz	V _{dd} = 2.5 V		350		uA
			V _{dd} = 3.0 V		450		
			V _{dd} = 5.0 V		800		
Twdt	The basic WDT time-out cycle time	V _{dd} = 2.5 V			24.3		mS
		V _{dd} = 3.0 V			22.3		mS
		V _{dd} = 4.0 V			19.6		mS
		V _{dd} = 5.0 V			17.9		mS
		V _{dd} = 5.5 V			17.4		mS



12. External Capacitor Selection For Crystal Oscillator

Osc. Type	Resonator Freq.	C1	C2
HF	20 MHz	5 pF ~10 pF	10 pF ~30 pF
	10 MHz	10 pF ~50 pF	20 pF ~100 pF
	4 MHz	10 pF ~50 pF	20 pF ~100 pF
XT	10 MHz	10 pF ~30 pF	10 pF ~50 pF
	4 MHz	10 pF ~50 pF	20 pF ~100 pF
	1 MHz	10 pF ~30 pF	20 pF ~50 pF
LF	1 MHz	3 pF ~5 pF	3 pF ~5 pF
	455 K	10 pF ~30 pF	20 pF ~50 pF
	32 K	10 pF ~20 pF	15 pF ~30 pF



喬懌電子科技股份有限公司

Chau Yi In Circuit Design Technology Co., Ltd

5F.-3, No.678, Sec. 4, Bade Rd., Songshan Dist., Taipei City Taiwan (R.O.C.)

Tel:886-2-27626188 Fax: 886-2-87870579

Attn: Judy